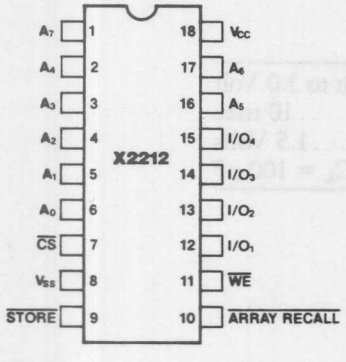
PRELIMINARY DATA SHEET
Characteristics Subject to Change
Without Notice.

256 x 4 Bit Nonvolatile Static RAM
5V-Programmable
X2212-30

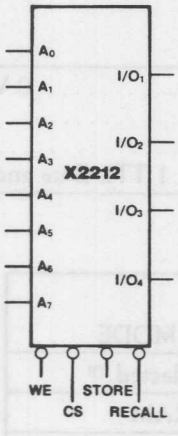
- **NONVOLATILE STATIC RAM:** The **X2212** contains 2K bits of memory organized as a conventional 1K static RAM overlaid bit-for-bit with a nonvolatile 1K Electrically Erasable PROM (E^2PROM). Nonvolatile data can be stored in the E^2PROM and at the same time independent data can be accessed in the RAM memory. At any time, data can be transferred back-and-forth between the RAM and E^2PROM by simple store and array recall signals.
- **5V-PROGRAMMABLE:** High-voltage pulses or supplies are never required. A single 5V supply is the *only power source* ever required for any function.
- **EASE-OF-USE:** Unprecedented simplicity, all inputs and outputs are directly TTL compatible. Fully static timing. 18-pin package.
- **PERFORMANCE:** RAM cycle time is less than 300 ns. During the lifetime of the device, data can be recalled from the E^2PROM an unlimited number of times.
- **POWER-FAILURE PROTECTION:** One simple TTL signal saves the entire RAM database. A snapshot nonvolatile copy of all RAM data is internally stored safe without power and can be recalled to the RAM when power returns. No battery backup required.
- **ORGANIZED FOR MICROCOMPUTER SYSTEMS:** The common data input and output is organized four bits wide.

Xicor's X2212 is fabricated with reliable n-channel floating gate MOS technology. For systems where RAM nonvolatility or *in-the-circuit* ROM changes by TTL signals are important, the **Xicor X2212** is an ideal choice.

PIN CONFIGURATION
18 PIN DIP .300"



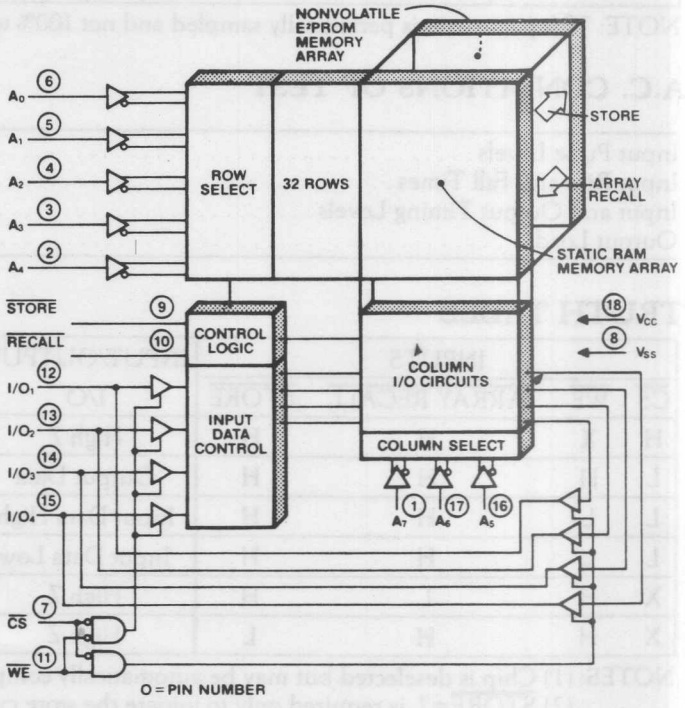
LOGIC SYMBOL



PIN NAMES

A_0–A_7	ADDRESS INPUTS
I/O_1–I/O_4	DATA INPUT/OUTPUT
$\overline{WE}$	WRITE ENABLE
$\overline{CS}$	CHIP SELECT
$\overline{ARRAY\ RECALL}$	ARRAY RECALL
$\overline{STORE}$	STORE
V_{CC}	+5V
V_{SS}	GROUND
NC	NO CONNECT

FUNCTIONAL DIAGRAM X2212 (256 x 4)



Advanced data sheet effective March 1981 Revision B

XICOR, INC., 1221 Innsbruck Drive, Sunnyvale, California 94086 Telephone: (408) 734-3041 TWX: 910-379-0033

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... −10°C to +85°C
Storage Temperature ..... −65°C to +125°C
Voltage on Any Pin with
Respect to Ground ..... −1.0V to +6V
D.C. Output Current 5mA

***COMMENT**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

X2212 D.C. AND OPERATING CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = +5V ±5%, unless otherwise specified.

Symbol	Parameter	LIMITS Min	Typ (3)	Max	Units	Test Conditions
I_{CC}	Power Supply Current		40	55	mA	All Inputs = 5.25V $I_{I/O}$ = 0mA T_A = 0°C
I_{LI}	Input Load Current		.1	10	µA	V_{IN} = GND to 5.25V
I_{LO}	Output Leakage Current		.1	10	µA	V_{OUT} = GND to 5.25V
V_{IL}	Input Low Voltage	−1.0		.8	V	
V_{IH}	Input High Voltage	2.0		V_{CC}	V	
V_{OL}	Output Low Voltage			.4	V	I_{OL} = 4.2mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = −2mA

CAPACITANCE

T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V

Symbol	Test	Max	Unit	Conditions
$C_{I/O}$	Input/Output Capacitance	5	pF	$V_{I/O}$ = 0V
C_{IN}	Input Capacitance	5	pF	V_{IN} = 0V

NOTE: This parameter is periodically sampled and not 100% tested.

A.C. CONDITIONS OF TEST

Input Pulse Levels ..... 0 Volt to 3.0 Volt
Input Rise and Fall Times ..... 10 nsec
Input and Output Timing Levels ..... 1.5 Volts
Output Load ..... 1 TTL Gate and C_L = 100 pF

TRUTH TABLE

INPUTS				INPUT/OUTPUT	
$\overline{CS}$	$\overline{WE}$	$\overline{ARRAY\ RECALL}$	$\overline{STORE}$	I/O	MODE
H	X	H	H	High Z	Not Selected (1)
L	H	H	H	Output Data	Read RAM
L	L	H	H	Input Data High	Write "1" RAM
L	L	H	H	Input Data Low	Write "0" RAM
X	H	L	H	High Z	Array Recall
X	H	H	L	High Z	Nonvolatile Storing (2)

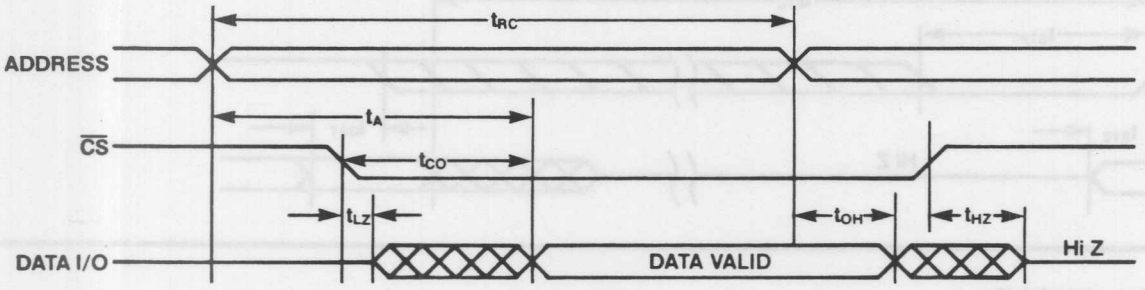
NOTES: (1) Chip is deselected but may be automatically completing a store cycle.
(2) $\overline{STORE}$ = L is required only to initiate the store cycle, after which the store cycle will be automatically completed ($\overline{STORE}$ = X).

X2212 A.C. CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = +5V ±5%, unless otherwise specified.

READ CYCLE

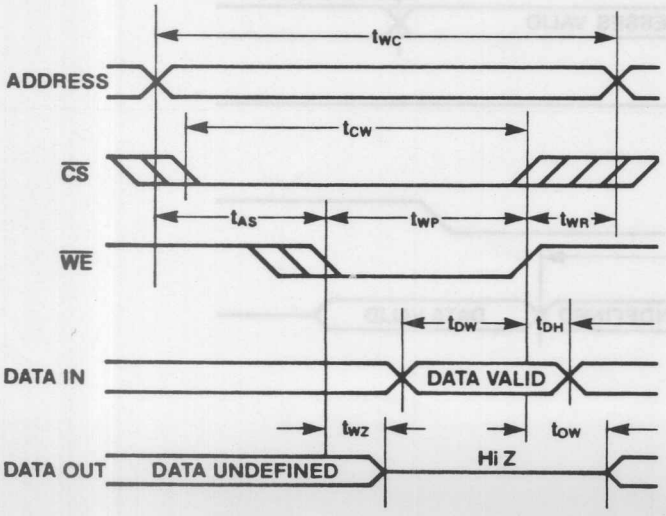
Symbol	Parameter	LIMITS Min	Typ[3]	Max	Units
t_{RC}	Read Cycle Time	300			ns
t_A	Access Time			300	ns
t_{CO}	Chip Select to Output Valid			200	ns
t_{OH}	Output Hold from Address Change	50			ns
t_{LZ}	Chip Select to Output in Low Z	10			ns
t_{HZ}	Chip Deselect to Output in High Z	10		100	ns



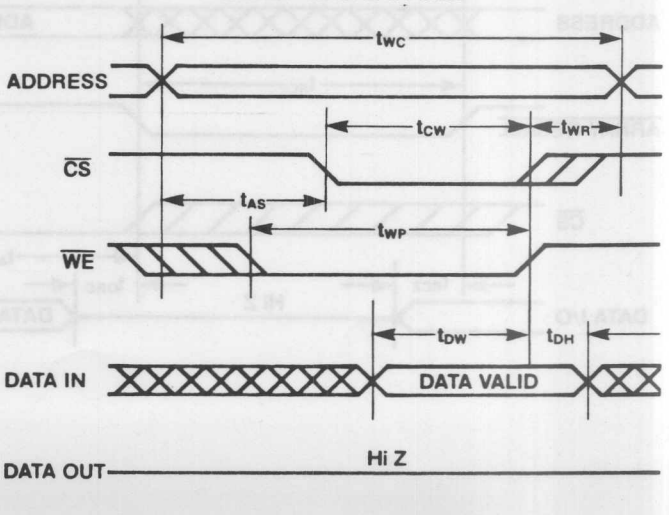
WRITE CYCLE

Symbol	Parameter	LIMITS Min	Typ[3]	Max	Units
t_{WC}	Write Cycle Time	300			ns
t_{CW}	Chip Select to End of Write	150			ns
t_{AS}	Address Set-up Time	50			ns
t_{WP}	Write Pulse Width	100			ns
t_{WR}	Write Recovery Time	25			ns
t_{DW}	Data Valid to End of Write	100			ns
t_{DH}	Data Hold Time	20			ns
t_{WZ}	Write Enable to Output in High Z	10		100	ns
t_{OW}	Output Active from End of Write	10			ns

WRITE CYCLE



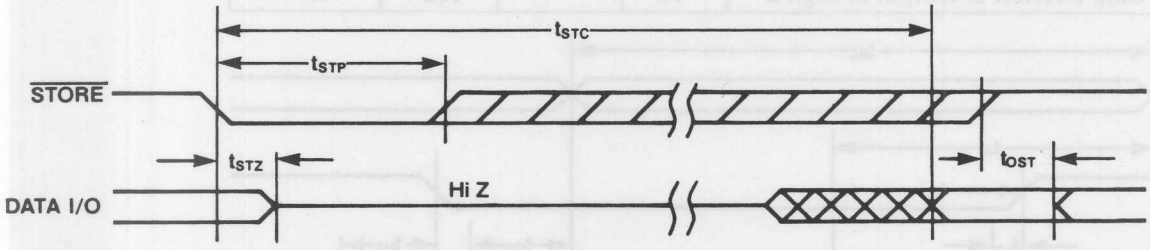
EARLY WRITE CYCLE



STORE CYCLE

Symbol	Parameter	LIMITS Min	Typ(3)	Max	Units
t_{STC}	Store Cycle Time			10	ms
t_{STP}	Store Pulse Width	100			ns
t_{STZ}	Store to Output in High Z			100	ns
t_{OST}	Output Active from End of Store	10			ns

NUMBER OF STORE CYCLES: Based on presently available data, the X2212 is expected to perform typically 5,000 valid store cycles. A minimum number of 1,000 valid store cycles is specified.

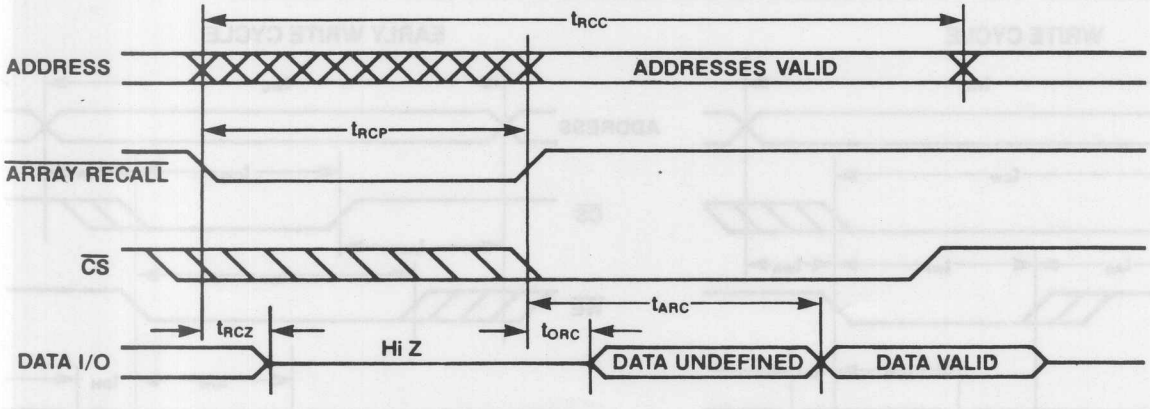


ARRAY RECALL CYCLE

Symbol	Parameter	LIMITS Min	Typ(3)	Max	Units
t_{RCC}	Array Recall Cycle Time	1500	1000		ns
t_{RCP}	Recall Pulse Width	750			ns
t_{RCZ}	Recall to Output in High Z			100	ns
t_{ORC}	Output Active from End of Recall	10			ns
t_{ARC}	Recalled Data Access Time from End of Recall			600	ns

NUMBER OF RECALL CYCLES: After data has been stored properly in the nonvolatile memory (E^2PROM), the X2212 is expected to recall this data an unlimited number of times during the lifetime of the device.

NOTE: (3) Typical values are for $T_A = 25°C$ and nominal supply voltages.



X2212 DEVICE OPERATION

ADDRESSES (A_0-A_7):

The eight address inputs select one of the 256 4-bit words.

CHIP-SELECT ($\overline{CS}$):

The chip select terminal affects the data-in/data-out and write enable terminals. When chip-select is high, the I/O terminals are in the floating or high impedance state.

WRITE ENABLE ($\overline{WE}$):

RAM READ/WRITE CYCLES

The RAM read or RAM write mode is selected through the write enable terminal when $\overline{CS}$ is low. A logic high selects the RAM read mode; a logic low selects the RAM write mode.

STORE ($\overline{STORE}$):

NONVOLATILE E²PROM WRITE CYCLE

Modification of data in the E²PROM memory is controlled by the $\overline{STORE}$ terminal. A low logic $\overline{STORE}$ signal applied to a device defines a store cycle which transfers a complete 256 x 4-bit copy of all 256 x 4-bit RAM storage locations into the corresponding 1024-bit locations of the overlaid nonvolatile E²PROM memory. The data in the E²PROM has been modified and is a "snapshot copy" of the current RAM data. The original data in the RAM remains valid. A low logic $\overline{STORE}$ signal initiates an automatic internal store operation. A low logic $\overline{STORE}$ into a device also inhibits write enable and array recall: data-in/data-out terminals are in a high impedance state. The inhibited terminals are enabled by either automatic completion of the internal store operation or upon a high logic $\overline{STORE}$, whichever is longer. A store cycle can take place when $\overline{CS}$ is high or low. Data stored in the E²PROM remains valid with or without power supplied.

Care must be taken to prevent an unintentional initiation of a store cycle during power-up and power-down. A low logic $\overline{ARRAY\ RECALL}$ will inhibit the initiation of a $\overline{STORE}$ operation. In many microcomputer systems the system reset command can be used during power-up and power-down to generate a low $\overline{ARRAY\ RECALL}$. Another means of assuring a store cycle will not be initiated during power-up or power-down is to keep $\overline{STORE}$ high, for example by tying the input through a pullup resistor to V_{CC}, to assure that $\overline{STORE}$ approximately equals V_{CC}. In addition, the $\overline{STORE}$ operation is inhibited for V_{CC} approximately less than 3 volts.

ARRAY RECALL ($\overline{ARRAY\ RECALL}$):

NONVOLATILE E²PROM READ CYCLE

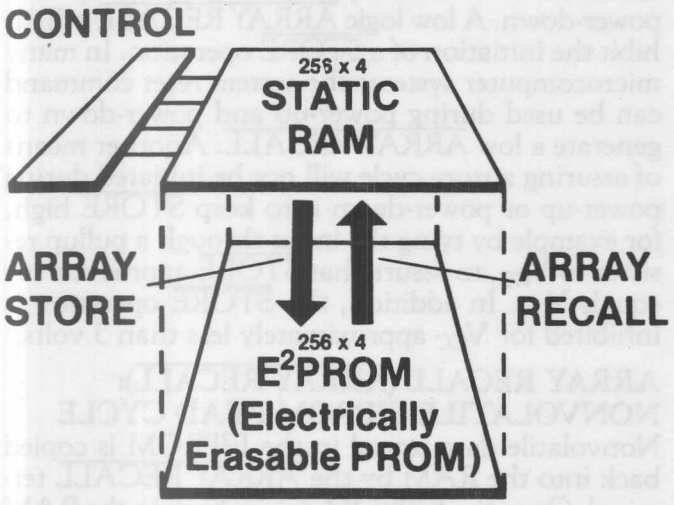
Nonvolatile data stored in the E²PROM is copied back into the RAM by the $\overline{ARRAY\ RECALL}$ terminal. Once the E²PROM data is back in the RAM it can then be accessed by normal RAM read or write cycles. A low logic $\overline{ARRAY\ RECALL}$ into a device initiates a cycle that in a single operation transfers the entire 1024-bit E²PROM array data bit-for-bit into the 1024-bit RAM memory. The E²PROM data overwrites any data then existing in the RAM at the beginning of an $\overline{ARRAY\ RECALL}$ cycle. The data in the E²PROM remains unaltered.

A low logic $\overline{ARRAY\ RECALL}$ inhibits the $\overline{STORE}$ terminal. An array recall cycle can take place when $\overline{CS}$ is high or low.

DATA-IN/DATA-OUT (I/O_1-I/O_4):

Data can be written into the RAM section of a selected device when the write enable input is low. The three-state output buffer provides direct TTL compatibility. The I/O terminals are in the high impedance state when chip select is high or whenever a write operation is being performed.

MEMORY ORGANIZATION



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Purchaser is solely responsible to determining whether any Xicor product is suitable for use in purchaser's application. Xicor therefore assumes no responsibility for purchaser's circuits and systems operation.

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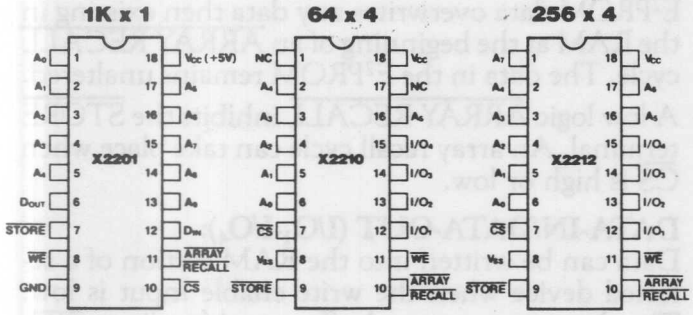

A GROWING FAMILY OF NONVOLATILE STATIC RAMS

Available for immediate delivery, the X2201 is the first single 5V supply nonvolatile static RAM and is organized 1K x 1 bits. To meet the further needs of many microcomputer based systems two new nonvolatile RAMs complement the X2201. The X2210 is organized 64 x 4 bits; the X2212 is organized 256 x 4 bits. For maximum system design flexibility, the X2210 and X2212 have compatible pin-outs and can be exchanged in the same 18-pin socket.